IN-SITU DOPING OF ARSENIC FOR SOURCE AND DRAIN EPITAXY

BACKGROUND

The source and drain regions of n-type metal-oxide-semiconductor (NMOS) field-effect transistors (FETs) need to have n-type impurities. The commonly used n-type impurities include phosphorous and arsenic. Conventionally, when arsenic is doped, it is implanted into the source and drain regions, for example, by using AsH_3 as the dopant-containing process gas.

The implanted arsenic, however, is not activated. To cure the implanted arsenic, and also to cure the crystalline structure in the source and drain regions, thermal processes are necessary. The thermal processes cause the undesirable dopant diffusion, which leads to the loss of junction abruptness. Furthermore, the thermal processes also cause thermal budget issues in the manufacturing of the integrated circuits.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the embodiments, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

FIGS. **1** through **9** are cross-sectional views of intermediate stages in the manufacturing of an n-type metal-oxide-semiconductor (NMOS) fin field-effect transistor (FinFET) in accordance with embodiments; and

FIGS. **10** and **11** are cross-sectional views of intermediate stages in the manufacturing of a planar n-type FET in accordance with alternative embodiments.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

The making and using of the embodiments of the disclosure are discussed in detail below. It should be appreciated, however, that the embodiments provide many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative, and do not limit the scope of the disclosure.

An n-type metal-oxide-semiconductor (NMOS) field-effect transistor (FET) and the method of forming the same are provided in accordance with embodiments. The intermediate stages of manufacturing various embodiments are illustrated. The variations of the embodiments are discussed. Throughout the various views and illustrative embodiments, like reference numbers are used to designate like elements.

Referring to FIG. **1**, substrate **20**, which may be a portion of a semiconductor wafer, is provided. Substrate **20** may be a semiconductor substrate. In an embodiment, substrate **20** is a silicon substrate with no germanium therein, although it may also be formed of silicon germanium (SiGe). Insulators such as shallow trench isolation (STI) regions **22** are formed in substrate **20**. Depth D**1** of STI regions **22** may be between about 50 nm and about 300 nm, or between about 100 nm and about 400 nm. It is realized, however, that the dimensions recited throughout the description are merely examples, and may be changed to different values. STI regions **22** may be formed by recessing semiconductor substrate **20** to form openings, and then filling the openings with dielectric materials. STI regions **22** may include two neighboring regions having their sidewalls facing each other, with a portion of substrate **20** between, and adjoining, the two neighboring STI regions **22**.

Referring to FIG. **2**, the portion of substrate **20** that is between two neighboring STI regions **22** is removed, forming opening **24**. In an embodiment, the bottom of opening **24** is level with the bottoms of STI regions **22**. In alternative embodiments, the bottom of opening **24** may be lower than or higher than the bottoms of STI regions **22**.

FIG. **3** illustrates the formation of SiGe layer **26** in opening **24**. The methods for forming SiGe layer **26** include, for example, selective epitaxial growth (SEG). SiGe layer **26** may be expressed as $Si_{1-x}Ge_x$, wherein x is the atomic percentage of germanium, and x is greater than 0, and may be equal to or less than 1. When x is equal to about 1, SiGe layer **26** is formed of substantially pure germanium. In an exemplary embodiment, x is between about 0.5 and about 1.0. SiGe layer **26** may be fully relaxed regardless of the material and the structure of substrate **20**.

In FIG. **4**, semiconductor layer **28** is epitaxially grown on SiGe layer **26**. In an embodiment, semiconductor layer **28** is formed of silicon germanium, which may be expressed as $Si_{1-y}Ge_y$, wherein value y is the atomic percentage of germanium in the silicon germanium, and value y may be greater than or equal to 0, and is less than 1. Atomic percentage y of semiconductor layer **28** may be smaller than atomic percentage x of silicon germanium layer **26**. In an exemplary embodiment, atomic percentage y is between about 0 and about 0.7. In other embodiments, semiconductor layer **28** is formed of substantially pure silicon. In yet other embodiments, semiconductor layer **28** may include a III-V compound semiconductor that comprises a group-III element and a group-V element. The III-V compound semiconductor may include, but is not limited to, GaAs, InP, GaN, InGaAs, InAlAs, GaSb, AlSb, AlAs, AlP, GaP, combinations thereof, and multi-layers thereof. Semiconductor layer **28** may have a lattice constant smaller than the lattice constant of silicon germanium layer **26**. Accordingly, a tensile stress may be generated in semiconductor layer **28**.

Referring to FIG. **5**A, STI regions **22** are recessed, so that top surface **28**A of semiconductor layer **28** is higher than top surfaces **22**A of the remaining portions of STI regions **22**. In an embodiment, top surfaces **22**A may be at an intermediate level that is between top surface **28**A and bottom surface **28**B of semiconductor layer **28**. In alternative embodiments, top surfaces **22**A may be level with, or lower than, bottom surface **28**B. Throughout the description, the portion of semiconductor layer **28** (and possibly SiGe layer **26**) that are over top surfaces **22**A is referred to as fin **30**. Fin **30** has fin height H. In an exemplary embodiment, fin height H is between about 10 nm and about 50 nm. FIG. **5**B illustrates a cross-sectional view of the structure shown in FIG. **5**A, wherein the cross-sectional view is obtained from the vertical plane crossing line **5**B-**5**B in FIG. **5**A.

FIGS. **6**A and **6**B illustrate the formation of gate dielectric **32**, gate electrode **34**, and gate spacers **36**. Referring to FIG. **6**A, gate dielectric **32** is formed on the sidewalls and the top surface of fin **30**. The material of gate dielectric **32** may include silicon oxide, silicon nitride, high-k dielectric materials such as Hf-containing dielectrics, and the like. Gate electrode **34** may be formed of polysilicon, metals, metal silicides, and/or the like. FIG. **6**B is a cross-sectional view of the structure shown in FIG. **6**A, wherein the cross-sectional view is obtained from the vertical plane crossing line **6**B-**6**B in FIG. **6**A. Gate spacers **36** are formed on the sidewalls of gate electrode **34**. In FIG. **6**B, dotted lines are used to illustrate the portions of gate dielectric **32** and gate electrode **34**